REMARKS

Claims 1-54 are pending in this application. Claims 1, 2, and 45 have been examined. Claim 1 is independent.

Request for Examination of Non-Elected Claims

Because claims 1 and 2 are generic, if they are found allowable, Applicant requests that the claims for non-elected species be examined as well.

Claim Rejection – 35 USC 102

Claims 1, 2, and 45 have been rejected under 35 U.S.C. 102(b) as being anticipated by Otsuka (U.S. Patent 6,021,071). Applicant respectfully traverses this rejection.

Applicant submits that Otsuka does not anticipate the present claimed invention. In particular, Applicant submits that Otsuka does not teach or suggest at least an amplifying transistor which amplifies an input signal, and a current path control section which controls a path of a current through the amplifying transistor.

The Office Action states that Otsuka's output circuit 10 teaches the claimed amplifying transistor, that Otsuka's power supply potential Vcc teaches the claimed input signal that is amplified by the amplifying

transistor, and that Otsuka's control circuit 20 teaches the claimed current path control section. Applicant disagrees.

Otsuka is directed to an output circuit, in a semiconductor IC, which has a programmable impedance control function to adjust output impedance. The output circuit (e.g., shown in Figure 2) has a programmable impedance buffer function to adjust the impedance of the output driving transistor to a desired value by varying the size of the output driving transistor through 4-bit control signals. The output circuit includes an offset transistor Tro, fine adjustment transistors Tro 1 to Tro 6, and transistors Tr1 to Tr5 having different sizes increasing in progression. The connection of the 4-bit control signals C0 to C3 to the transistors TR1 to Tr5 is changed using the option lines 11a so that channel width W of the output driving transistor can be fine adjusted in a wide control range. Column 10, lines 49 to 62.

Otsuka's output circuit does appear to change the size of the output driving transistor for impedance control. However, Otsuka's power supply potential Vcc is for setting all fine adjustment transistors Tro1 to Tro6 into the use state (column 9, lines 19-24). Otsuka's control circuit outputs 4-bit control signals so that width W of the output driving transistor can be fine adjusted. With respect to transistors Tr1 to Tr4 shown in Otsuka's figure 2, for example, the drains/current paths are

connected to an external node via output pad DQ. The sources are connected to a ground potential Vss. The gates are connected to respective control signals.

Therefore, unlike Otsuka, the present invention's input signal is amplified by the amplifying transistor. Also, unlike Otsuka, the present invention's current path control section controls the size of the input signal amplifying transistor and the path of the current through the amplifying transistors.

With respect to claim 2, Applicant disagrees that it would be inherent in Otsuka to include a current control transistor in its control circuit. Otsuka's control circuit controls transistor size by supplying control signals to the gates of the transistors. There is no suggestion in Otsuka that the control signals are supplied by a control transistor. Furthermore, since there is no current flowing through Otsuka's transistors, there can be no control of such current flow. Thus, Otsuka does not teach or suggest the structure of claim 2.

With respect to claim 45, because Otsuka does not teach a current flow through the amplifying transistor, it does not teach control and maintenance of current flow through the transistor at a constant level.

Thus, Applicant submits that Otsuka fails to teach or suggest each and every claimed element. Accordingly, Applicant requests that the rejection be withdrawn.

CONCLUSION

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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